**ECE 3457**

**Lab 2: nMOS Inverters**

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**Goal:**

Study nMOS inverters.

**Task A:**

Measure and plot the IV characteristics of a CD4007 enhancement-type nMOS transistor. Determine the threshold voltage, VT, and the conductivity parameter, K*.* As this was done in lab 1, we will use the calculated VT and K from Lab 1.

**Task B:**

Design, build and simulate a 10 kΩ resistively loaded nMOS inverter. Use VDD = 5 V. (1) Plot the load line and show intersections with the device IV curves (based on the measured VT and K). (2) Compute the VTC and plot results. (3) Measure the VTC and plot results. (4) Run simulation and show the simulated VTC.

**Task C:**

Repeat Task B using an enhancement-load nMOS inverter.

**Theory:**

From Lab 1: (Task A)

The CD4007 enhancement nMOS and pMOS transistors have gate, drain, and source pins. The transistor has the equations

for when the transistor is operating in the triode region (VGS > VT and VDS ≤ VGS – VT) and

for when the transistor is operating in the saturation region (VGS > VT and VDS > VGS – VT). As the transistor enters the saturation region, the ID curve will begin to plateau. This is because the equation for current through the drain and source pins is not dependent on VDS when the transistor is operating in the saturation region. By obtaining the nMOS and pMOS transistors’ iv curves for different VGS values, it becomes possible to derive the value of K where

We can calculate the value of K and VT by plotting the square root of IDS against VGS according to the linear equation

Where the square root of K is the slope and VT is the x-intercept.

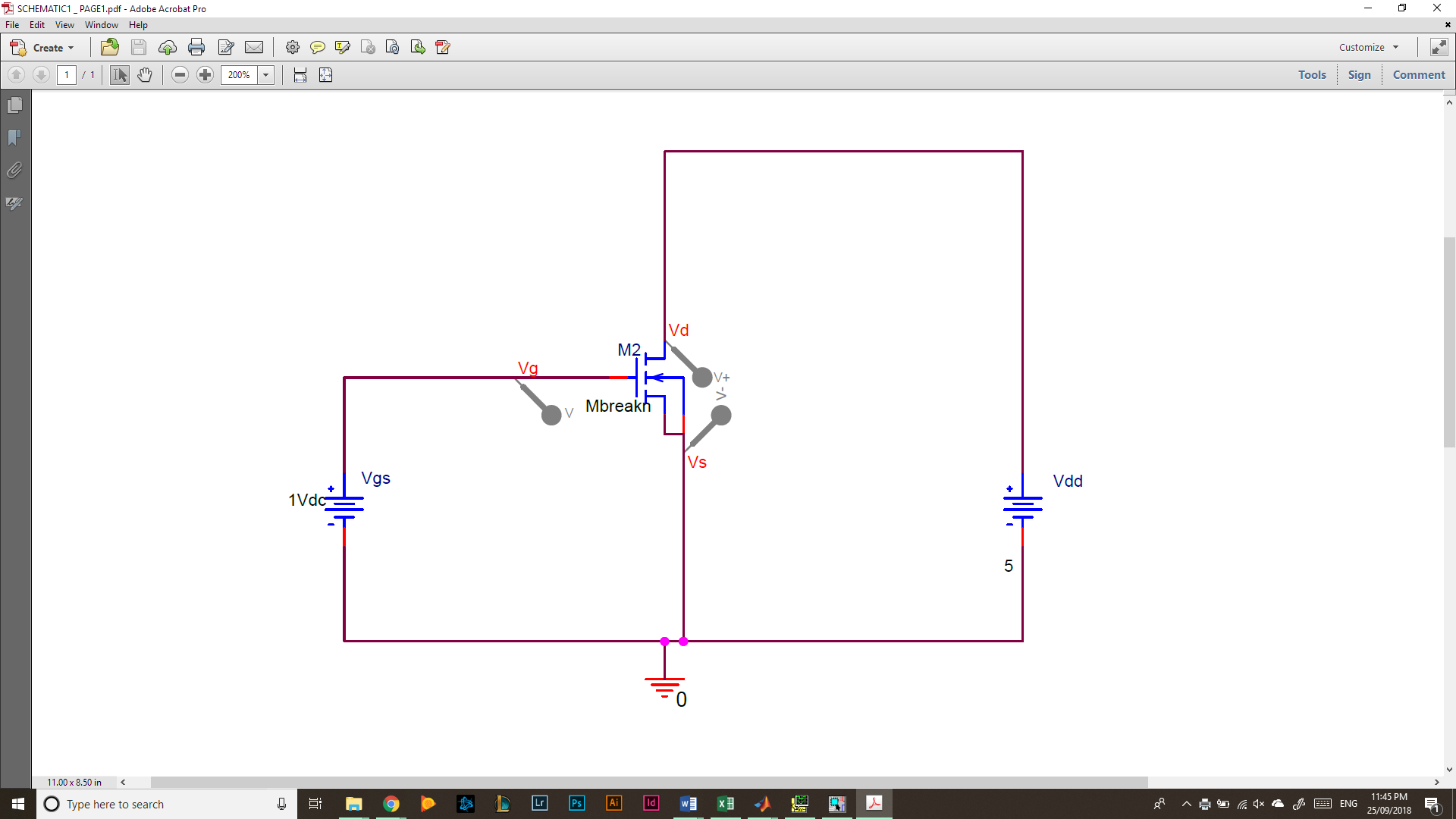
Lab 2: (Task B & C)

A transistor has 3 states: cutoff region, triode region, and saturation region. The transistor acts as an open circuit in the cutoff region, as such no current will flow. In the triode region, the current varies so the voltage across the transistor will also vary. When the transistor is operating in saturation mode, it’s current should no longer be changing dramatically so it acts like a small resistor, resulting in a small voltage reading across the transistor. As such the VTC for the resistively loaded nMOS inverter should have a VOH near VDD when Vin < VT. Similarly, the enhancement-load nMOS will be at VOH when Vin < VT but VOH will be closer to VDD – VT as the lower nMOS will be in cutoff region but still has a voltage across it. The saturation region will be the section of the curve with the most dramatic decrease in Vout with increasing Vin. And the triode region will be when the curves begin to plateau at their VOL levels.

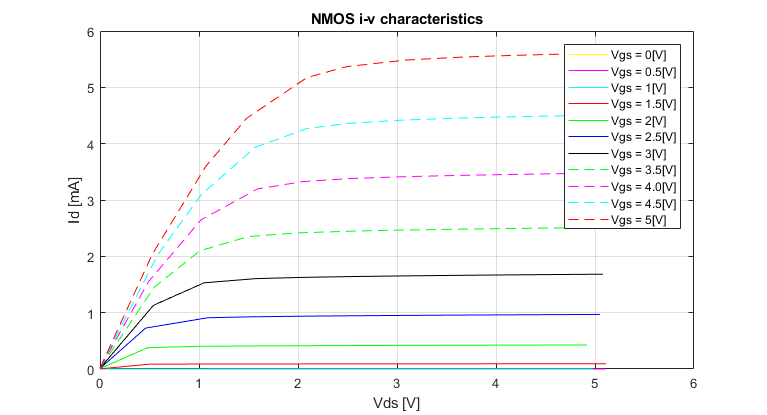
**Simulation & Experiment:**

**Task A: nMOS:**

The circuit was set up as below to test the iv characteristics of an enhancement nMOS.

  
*Figure 1: nMOS Test Circuit*

As in the above circuit, pin 3 was the gate voltage or VGS, pin 4 was the source voltage which was connected to ground, and pin 5 was the drain which was connected to VDS, or VDD according to Figure 1. Additionally, pin 7 (VSS) was connected to ground for proper operation of the chip. First VGS was set to 0 and then ID measured (the current through VD and VS) for VDD from 0[V] to 5[V] in 0.5[V] increments. Then VGS was incremented by 0.5[V] and the test for VDD and ID repeated. This process was repeated for VGS values from 0[V] to 5[V]. The following data was obtained for the nMOS transistor iv curves (tabular data at end of report).

  
*Figure 2: nMOS iv Characteristic Curves*

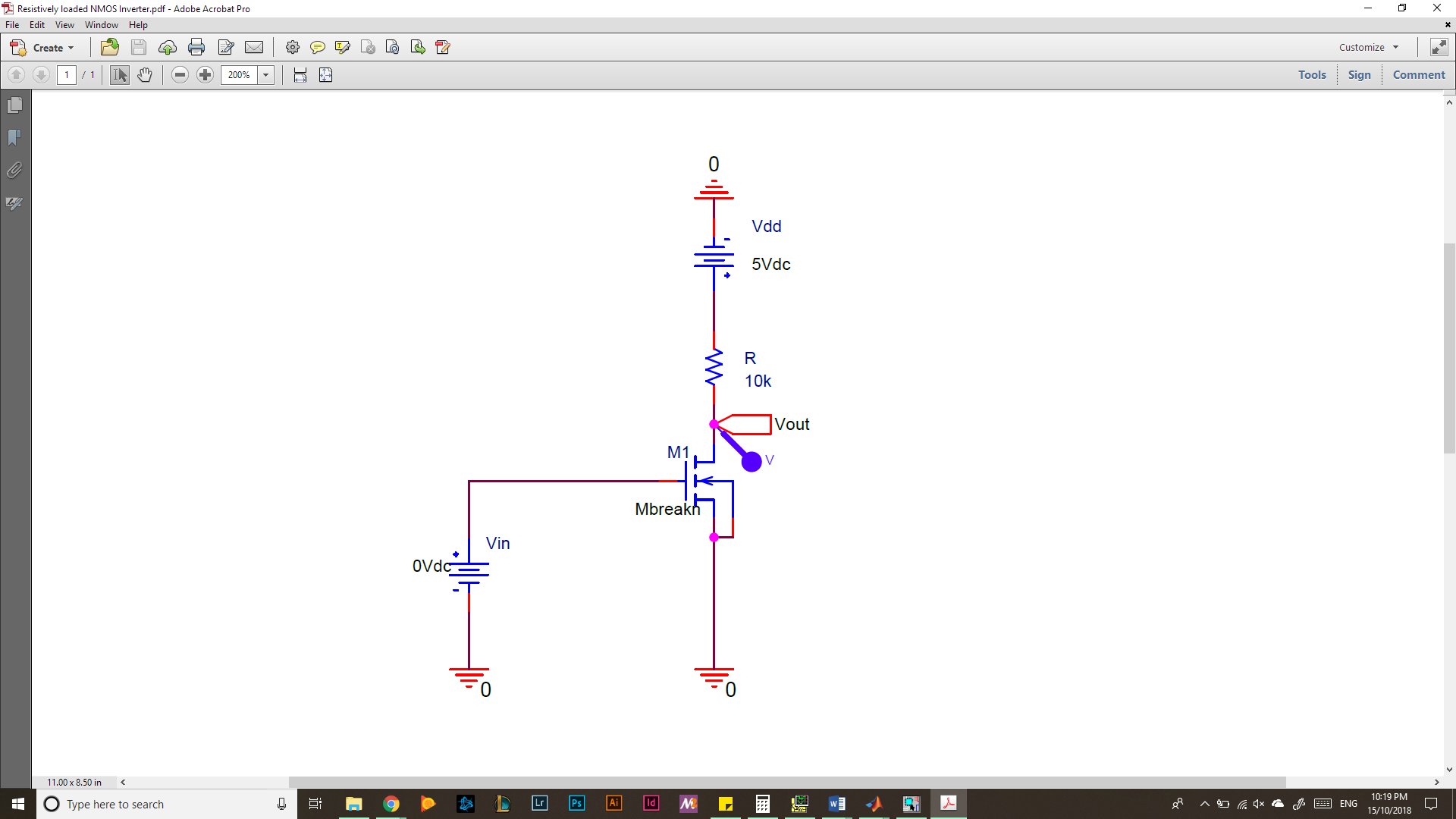
Values for K and VT can be found using this data. By selecting the current at which each transistor first enters saturation, or begins to plateau, a graph of the square root of ID vs VGS can be constructed. Currents that are consistently 0 across a VGS have been omitted.

*Figure 3: VGS vs ID1/2 For the nMOS Transistor*

The slope of this line is 0.018515 which is equivalent to the square root of K. Therefore, the value of K is 342.8[μA/V2], the value of Kn is 685.6[μA/V2], and the value of VT is obtained by setting y to 0 and solving for x. Therefore, VT is equal to 0.91[V].

**Task B: Resistively Loaded nMOS Inverter:**

The circuit below was used for Task B involving a resistively loaded nMOS Inverter.

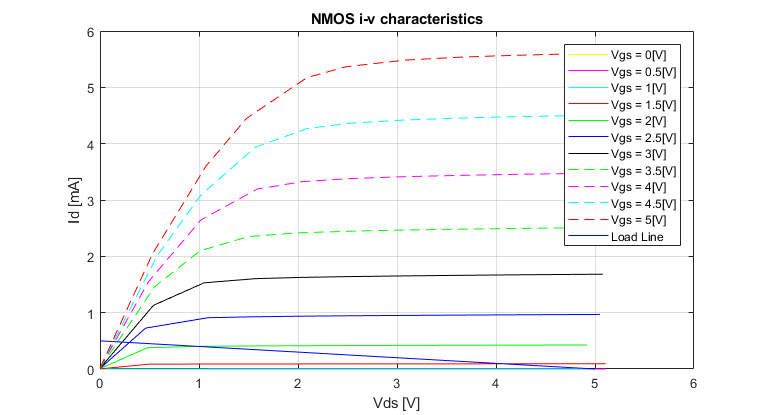


*Figure 4: Resistively Loaded nMOS Inverter Circuit*

VDD was set to a constant 5[V] and then Vin was incremented by 0.2[V] until it swept the voltage range from 0[V] to 5[V]. Vout was measured for each Vin value and the graph of Vin vs Vout was plotted to show the VTC.

1. **Graphical Analysis:**

The load line can be calculated using VDD and R. The theoretical highest current that could be provided by VDD and R alone is VDD/R = 0.5[mA] when VDS = 0[V]. Consequently, the minimum current will be when VDS = 5[V] such that there is no voltage across the resistor, so the current is 0. The nMOS iv characteristics graph with load line is included below.



*Figure 5: nMOS iv Characteristics with Load Line for Task B*

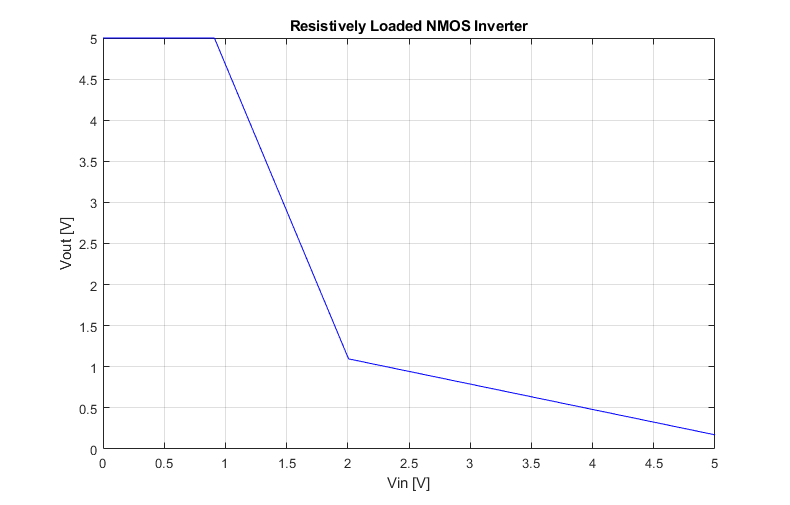
1. **Computed VTC**

By calculating some critical points for the voltage curve of the resistively loaded nMOS inverter, we can create a rough diagram of the VTC. The below diagram used points at edges of the graph and transition points between transistor operating modes. This means the points were 5[V] output for 0[V] input and consequently 5[V] output for 0.91[V] input for the cutoff region of operation. The values 1.0963[V] for output and 2.0063[V] for input were calculated for the point where the transistor switches from saturation to triode region of operation. This was done by solving simultaneously the equations

… (1)

Finally, the last point was found by using the value of 5[V] for Vin in the below equation

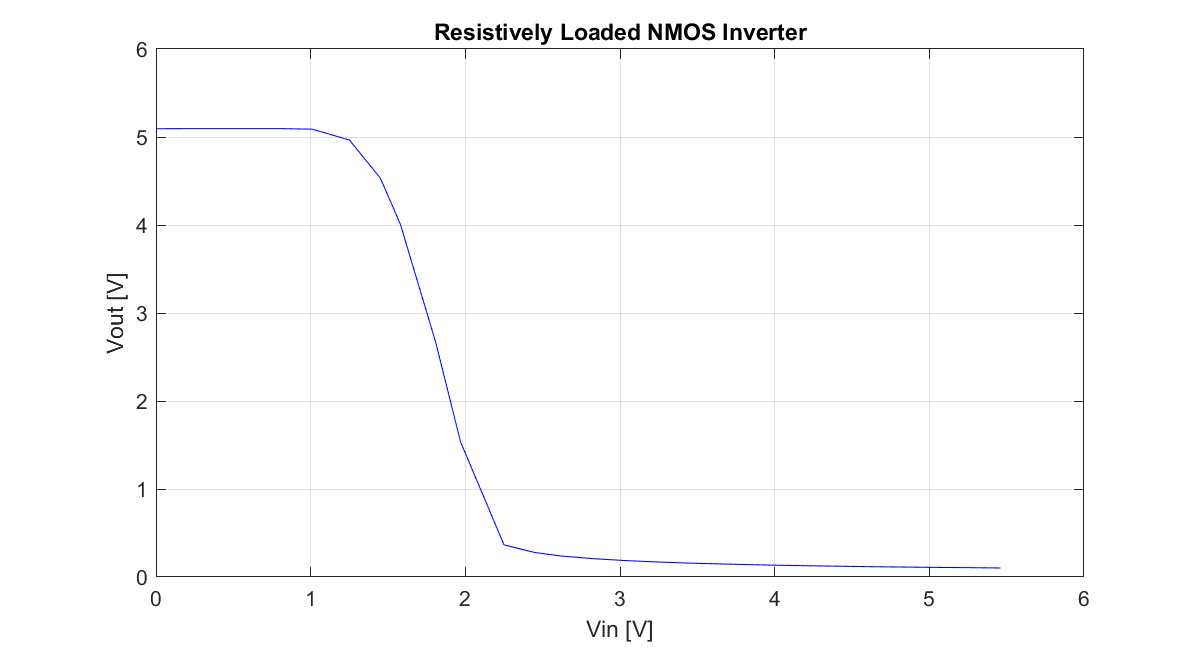
resulting in the point with Vout of 0.1723[V] for a Vin of 5[V].

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*Figure 6: Calculated Resistively Loaded nMOS Inverter VTC*

1. **Measured VTC**

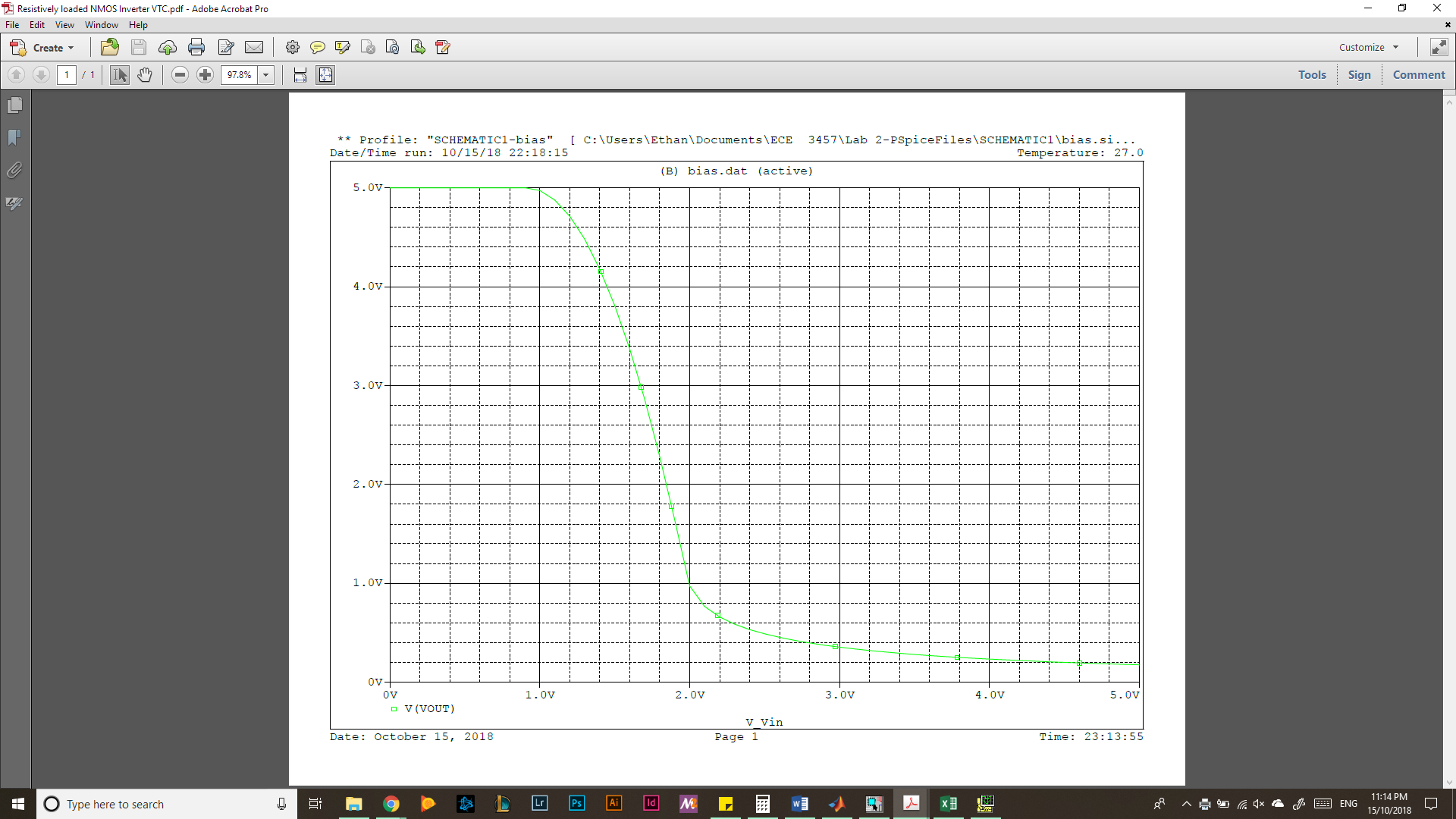
The data collected (see back pages) from the experiment set up according to Figure 4 is graphed below.



*Figure 7: Measured Resistively Loaded nMOS Inverter VTC*

1. **Simulated VTC**

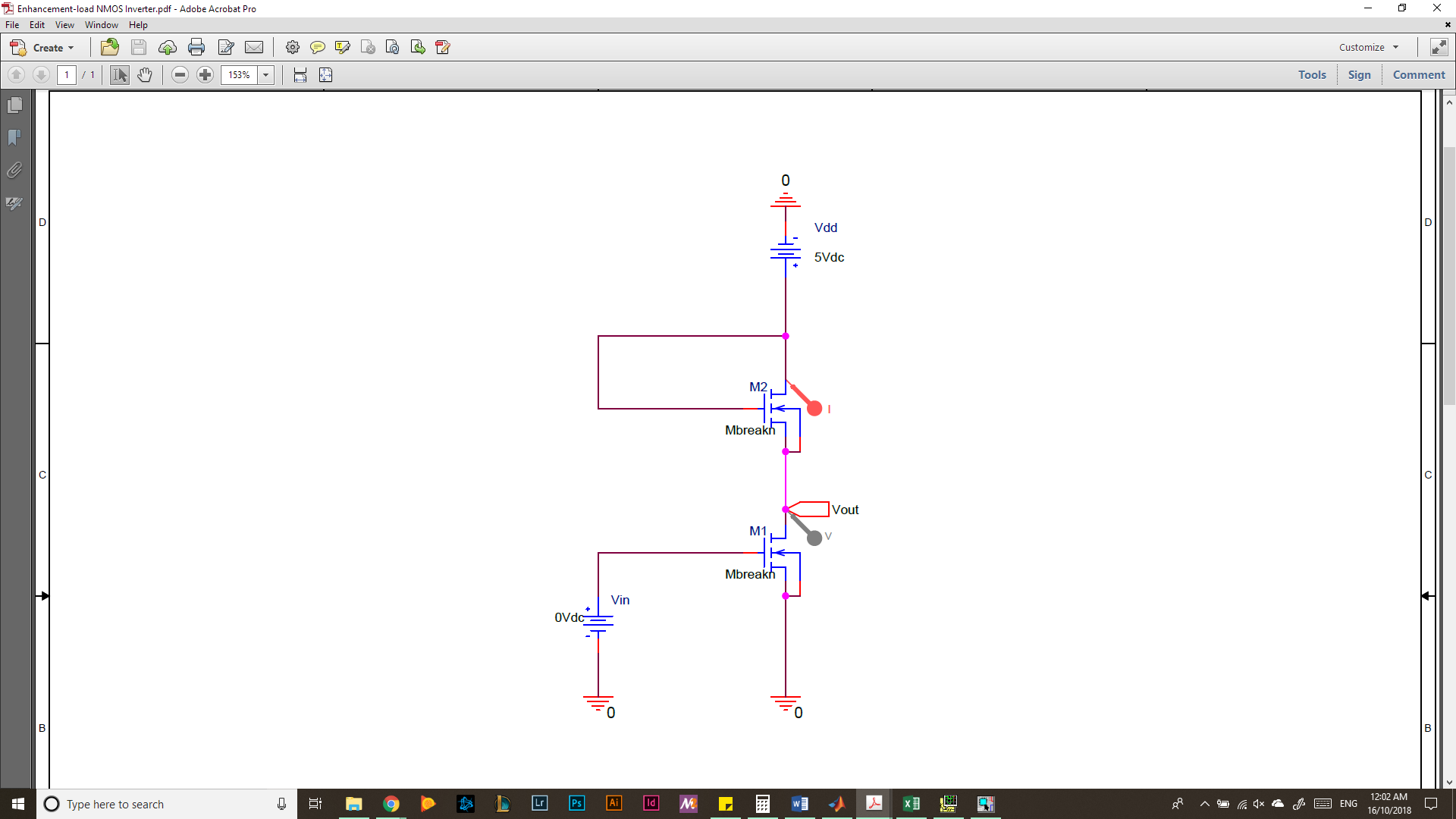
The circuit in Figure 4 was implemented in PSpice using VT of 0.91[V] and Kn of 685.6[μA/V2]. The following VTC was obtained for this circuit.



*Figure 8: Simulated VTC for Resistively Loaded nMOS Inverter*

**Task C: Enhancement-load nMOS Inverter**

The circuit below was used for Task C involving an enhancement-load nMOS inverter.



*Figure 9: Enhancement-load nMOS Inverter Circuit*

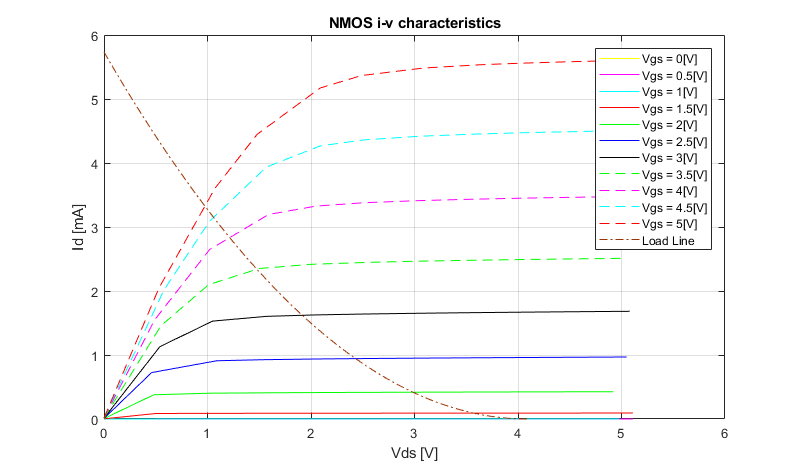
VDD was set to a constant 5[V] and then Vin was incremented by 0.2[V] until it swept the voltage range from 0[V] to 5[V]. Vout was measured for each Vin value and the graph of Vin vs Vout was plotted to show the VTC.

1. **Graphical Analysis:**

The load line can be easily calculated as the nMOS is always in the saturation region. Therefore, the lowest current will be 0 when VDS or Vout is greater than or equal to VDD -VT as this means that the bottom nMOS is operating in Cutoff region and the circuit is essentially open. The current will increase with the shape of a polynomial of degree 2 as VDS decreases, following the equation

where VDS < VDD – VT

The nMOS iv characteristics graph with load line is included below.



*Figure 10: nMOS iv Characteristics with Load Line for Task C*

1. **Computed VTC**

By calculating some critical points for the voltage curve of the enhancement-load nMOS inverter, we can create a rough diagram of the VTC. The below diagram used points at edges of the graph and transition points between the second transistor operating modes (the first transistor is always operating in saturation mode). This means the points were 4.09[V] output for 0[V] input and consequently 4.09[V] output for 0.91[V] input for the cutoff region of operation. This is because even though the second transistor is in the cutoff region, it still has a potential difference of VT across it. The values 2.045[V] for output and 2.955[V] for input were calculated for the point where the second transistor switches from saturation to triode region of operation. This was done by solving simultaneously the equations

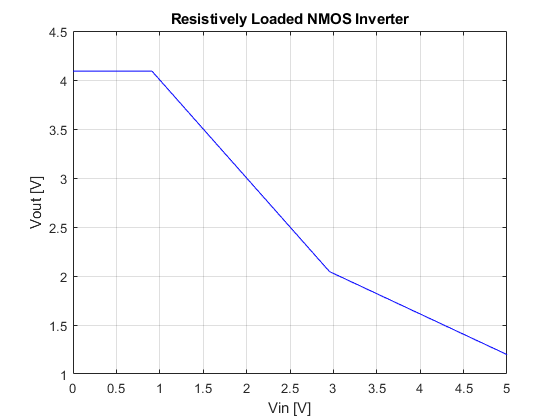
… (1)

… (2)

… (3)

Finally, the last point was found by using the value of 5[V] for Vin in the below equation

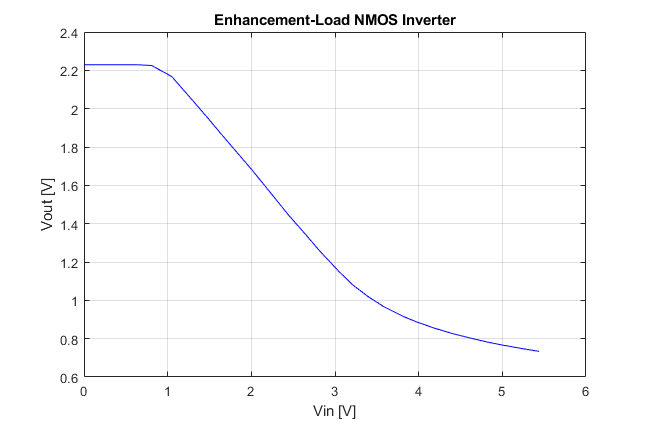
resulting in the point with Vout of 0.1723[V] for a Vin of 5[V].



*Figure 11: Calculated Enhancement-load nMOS Inverter VTC*

1. **Measured VTC**

The data collected (see back pages) from the experiment set up according to Figure 9 is graphed below.



*Figure 12: Measured Enhancement-load nMOS Inverter VTC*

1. **Simulated VTC**

The circuit was implemented in PSpice using the circuit in Figure 9 with a value VT of 0.91[V] and a Kn value of 685.6[μA/V2]. The following VTC was obtained for this circuit.



*Figure x: Simulated VTC for Enhancement-load nMOS Inverter*

**Analysis:**

The measured data matches the graphical analysis, calculated values, and simulation data in the case of the resistively loaded nMOS inverter from Task B. However, the measured data from Task C varies drastically from the values obtained from graphical analysis, computation of the VTC, and simulations of the circuit. While the circuit from Task B functioned according to expectations for all methods of analysis, Task C’s physical implementation did not behave as expected in theory. Task B’s behavior followed expectations with a cutoff region for Vin < VT and a VOH of ~5[V] across all testing. Similarly, the transistor transitioned from saturation state to triode state around Vin set to ~2[V]. Lastly, all curves had a similar VOL of ~0.2[V]. Task C differed in that all theory matched up to expectations, but the measured values for the circuit provided unexpected results. Which the shape was similar with the second transistor entering saturation and triode regions at the expected values of Vin but with unanticipated values of Vout. The measured VOH of ~2.2[V] was much lower than the expected value of ~4.1[V]. The measured VOL of ~0.75[V] at 5.0[V] Vin also did not match the expected VOL of ~1.2[V]. The discrepancies are due to a lack of complete understanding of the functionality of the CD4007 nMOS transistor chip. There is an issue with the way the circuit was designed using the chip.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| vGS [V] | **nMOS** | **Tabulated** | **Data** |  |  |  |  |  |  |  |  |  |
| 0 | vDS [V] | 0 | 0.51 | 1.09 | 1.59 | 2.08 | 2.48 | 2.96 | 3.49 | 4 | 4.55 | 5.03 |
|  | iD [mA] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0.5 | vDS (V) | 0 | 0.5 | 1 | 1.48 | 2.03 | 2.56 | 2.99 | 3.44 | 4.04 | 4.52 | 5.11 |
|  | iD (mA) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1 | vDS (V) | 0 | 0.49 | 1.09 | 1.64 | 2.01 | 2.64 | 3.1 | 3.56 | 4.02 | 4.51 | 4.98 |
|  | iD (mA) | 0 | 0.001 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1.5 | vDS (V) | 0 | 0.5 | 1.03 | 1.47 | 1.98 | 2.47 | 3.1 | 3.65 | 4.05 | 4.54 | 5.11 |
|  | iD (mA) | 0.0026 | 0.0861 | 0.0882 | 0.0891 | 0.0898 | 0.0906 | 0.0913 | 0.0919 | 0.0923 | 0.0927 | 0.0932 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2 | vDS (V) | 0 | 0.48 | 1.02 | 1.58 | 2.07 | 2.48 | 3.07 | 3.63 | 4.09 | 4.53 | 4.92 |
|  | iD (mA) | 0.0066 | 0.3781 | 0.4031 | 0.4095 | 0.4133 | 0.416 | 0.419 | 0.4216 | 0.4235 | 0.4251 | 0.4265 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2.5 | vDS (V) | 0 | 0.46 | 1.09 | 1.53 | 2.09 | 2.59 | 3.09 | 3.58 | 4.06 | 4.55 | 5.05 |
|  | iD (mA) | 0.0094 | 0.7257 | 0.91 | 0.9265 | 0.9383 | 0.9456 | 0.9515 | 0.9564 | 0.9607 | 0.9649 | 0.9687 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3 | vDS (V) | 0 | 0.54 | 1.05 | 1.57 | 2.05 | 2.51 | 3.05 | 3.48 | 4.03 | 4.47 | 5.08 |
|  | iD (mA) | 0.0123 | 1.1308 | 1.5297 | 1.604 | 1.6266 | 1.6402 | 1.6523 | 1.6602 | 1.669 | 1.6751 | 1.6829 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3.5 | vDS (V) | 0 | 0.55 | 1.01 | 1.5 | 1.99 | 2.58 | 3.01 | 3.58 | 4.03 | 4.57 | 5.01 |
|  | iD (mA) | 0.0142 | 1.457 | 2.0986 | 2.3515 | 2.416 | 2.449 | 2.4648 | 2.4808 | 2.4915 | 2.5022 | 2.5101 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 4 | vDS (V) | 0 | 0.49 | 1.02 | 1.59 | 2.05 | 2.51 | 3.03 | 3.51 | 4.04 | 4.52 | 4.99 |
|  | iD (mA) | 0.0165 | 1.5504 | 2.6471 | 3.1959 | 3.3268 | 3.3792 | 3.4115 | 3.4322 | 3.4504 | 3.4637 | 3.4752 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 4.5 | vDS (V) | 0 | 0.58 | 1.02 | 1.57 | 2.09 | 2.51 | 3.06 | 3.58 | 4.06 | 4.49 | 5.13 |
|  | iD (mA) | 0.0181 | 2.0178 | 3.0908 | 3.9378 | 4.2673 | 4.361 | 4.419 | 4.4515 | 4.4735 | 4.4884 | 4.5085 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 5 | vDS (V) | 0 | 0.53 | 1.07 | 1.48 | 2.09 | 2.49 | 3.09 | 3.64 | 4.04 | 4.51 | 4.99 |
|  | iD (mA) | 0.015 | 2.043 | 3.6003 | 4.449 | 5.1728 | 5.3674 | 5.4843 | 5.5355 | 5.56 | 5.5832 | 5.6018 |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Resistively** | | **Loaded** | **nMOS** | **Inverter** |  |  |  |  |  |  |  |  |  |
| Vin [V] | 0 | 0.24 | 0.43 | 0.56 | 0.81 | 1.01 | 1.25 | 1.45 | 1.58 | 1.81 | 1.97 | 2.25 | 2.45 | 2.62 |
| Vout [V] | 5.094 | 5.095 | 5.095 | 5.095 | 5.095 | 5.089 | 4.966 | 4.534 | 4.009 | 2.657 | 1.531 | 0.3654 | 0.2778 | 0.2385 |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 2.83 | 3.04 | 3.23 | 3.44 | 3.54 | 3.79 | 4 | 4.22 | 4.48 | 4.63 | 4.76 | 5.09 | 5.26 | 5.46 |
| 0.2081 | 0.1861 | 0.1714 | 0.1583 | 0.1534 | 0.1423 | 0.1343 | 0.1274 | 0.1208 | 0.1171 | 0.1144 | 0.1083 | 0.1062 | 0.1024 |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Enhancement-load** | | **nMOS** | **Inverter** |  |  |  |  |  |  |  |  |  |  |
| Vin [V] | 0 | 0.19 | 0.37 | 0.64 | 0.81 | 1.05 | 1.24 | 1.47 | 1.67 | 1.82 | 2.01 | 2.28 | 2.45 | 2.65 |
| Vout [V] | 2.229 | 2.229 | 2.229 | 2.229 | 2.225 | 2.167 | 2.072 | 1.956 | 1.852 | 1.776 | 1.679 | 1.534 | 1.442 | 1.343 |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 2.81 | 3.05 | 3.21 | 3.39 | 3.58 | 3.82 | 3.99 | 4.19 | 4.4 | 4.63 | 4.84 | 5.03 | 5.26 | 5.44 |
| 1.261 | 1.149 | 1.0815 | 1.0211 | 0.9675 | 0.9151 | 0.885 | 0.8546 | 0.827 | 0.8018 | 0.7804 | 0.7643 | 0.7464 | 0.7334 |